M.Tech
in
Electronics & Communication Engineering
w.e.f. 2011-2012

Deptt. of Electronics & Communication Engineering

Guru Jambheshwar University of Science & Technology, Hisar

First Semester

List of Compulsory/Core Courses

		Credits
ECL-712	IC Fabrication Technology	4
ECL-713	Digital VLSI Design	4
ECL-714	Hardware Description Languages	4
ECL-715	Embedded System Design	4
ECL-719	Signal Processing	4
ECP-716	Digital VLSI Design Lab	2
ECP-717	HDL Lab	2
ECP-718	Embedded System Design Lab	2
	Total Credits	26

Second Semester

List of Compulsory/Core Courses

		Credits
ECL-721	Mobile Communication	4
ECL-722	Advanced Optical Communication Systems	4
ECL-723	Analog IC Design	4
ECL-724	Adaptive Signal Processing	4
	Elective-I	4
ECP-726	Adaptive Signal Processing Lab	2
ECP-727	Advanced Communication Lab	2
	Total Credits	24

List of Electives -I: The student can opt any one elective from the following list.

ECL-725 (i)	Algorithms for VLSI Design Automation
ECL-725 (ii)	Advanced Computer Architecture
ECL-725 (iii)	MEMS and IC Integration

Third Semester

List of Compulsory/Core Courses

		Credits
	Elective-II	4
ECP -732	Advance VLSI Design Lab	2
ECP-733	Communication System Design Lab	2
ECD-730	Thesis – Part I with Seminar	3
	Total Credits	11

List of Electives- II: The student can opt one elective from the following list.

ECL-731 (i)	Mixed-Signal Design
ECL-731 (ii)	RF Micro-electronics
ECL-731 (iii)	VLSI Testing And Testability
ECL-731 (iv)	Memory System Design
ECL-731 (v)	Low Power VLSI Design
ECL-731 (vi)	Embedded System for Wireless & Mobile Communication
ECL-731 (vii)	Hardware & Software Co-Design
ECL-731 (viii)	Advanced Digital Communication
ECL-731 (ix)	Satellite Communication

Fourth Semester

		Credits
ECD-740	Thesis – Part II	09
	Total Credits	09

- 04 contact Hrs per week are required for each theory subject including electives.
- 04 contact Hrs per week are required for each Lab.
- 02 Hrs per student per week teaching load will be assigned for thesis work. for Part I and Part II.

Semester	**Total Credits**
I.	**26**
II.	**24**
III.	**11**
IV.	**09**
Grand Total	**70 Credits**

DETAILED SYLLABUS

M.Tech. (ECE)

FIRST SEMESTER

ECL-712	IC Fabrication Technology

Environment for VLSI Technology : Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterisation of Impurity profiles.

Oxidation : Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.

Lithography : Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapour Deposition techniques : CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology.

Metal film deposition : Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallisation schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Texts/References:

1. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1994(2nd Edition).
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
3. Plummer, Deal , Griffin "Silicon VLSI Technology: Fundamentals, Practice & Modeling" PH, 2001.
4. P. VanZant , "Microchip Fabrication", 5th Edition, MH , 2000.

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-713	Digital VLSI Design

1. Introduction to MOSFETs : MOS Transistor Theory - Introduction MOS Device, Fabrication and Modeling , Body Effect, Noise Margin; Latch-up

2. MOS Inverter : MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Static Load MOS Inverters, Transistor Sizing, Static and Switching Characteristics; MOS Capacitor; Resistivity of **V**arious Layers.

3. Symbolic and Physical Layout Systems -- MOS Layers Stick/Layout Diagrams; Layout Design Rules, Issues of Scaling, Scaling factor for device parameters.

4. Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.

5. Sequential MOS Logic Circuits: SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop.

6. Dynamic Logic Circuits; Basic principle, nonideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

7. CMOS Subsystem Design: Semiconductor memories, memory chip organization, RAM Cells, dynamic memory cell.

TEXT BOOKS:

1. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits : Analysis and Design*, Third Edition, MH, 2002.

REFERENCE BOOKS:

1. W. Wolf, *Modern VLSI Design : System on Chip*, Third Edition, PH/Pearson, 2002.
2. N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design : A Systems Perspective*, Second Edition (Expanded), AW/Pearson, 2001.
3. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson, 2003.
4. D. A. Pucknell and K. Eshraghian, *Basic VLSI Design : Systems and Circuits*, Third Edition, PHI, 1994.
5. J. P. Uyemura, *CMOS Logic Circuit Design*, Kluwer, 1999.
6. J. P. Uyemura, *Introduction to VLSI Circuits and System*, Wiley, 2002.
7. R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PH, 1997.

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ECL-714	Hardware Description Languages

1. **Introduction To Hardware Design:** Digital System Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction.
2. **VHDL Background:** VHDL History, Existing Languages, VHDL Requirements, The VHDL Language.
3. **Design Methodology Based On VHDL:** Elements of VHDL, Top down Design, Top down Design with VHDL, Subprograms, Controller Description, VHDL Operators, Conventions and Syntax.
4. **Basic Concepts In VHDL:** Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.
5. **Design Organization and Parameterization:** Definition and Usage of Subprograms, Packaging Parts and Utilities, Design Parameterization, Design Configuration, Design Libraries.
6. **Utilities For High-Level Descriptions:** Type Declarations and Usage, VHDL Operators, Subprogram Parameter Types and Overloading, Other Types and Type Related Issues, Predefined Attributes, User Defined Attributes.
7. **Dataflow Descriptions In VHDL:** Multiplexing and Data Selection, State Machine Description, Three State Bussing.
8. **Behavioral Description of Hardware:** Process Statement, Assertion Statement, Sequential Wait Statements, Formatted ASCII I/O Operations, MSI Based Design.
9. **Verilog:** Overview of Digital design with Verilog HDL, Hierarchical modeling concepts, basic concepts, modules & ports.

TEXT BOOKS:

1. J. Bhasker, *A VHDL Primer*, Third Edition, PH/Pearson, 1999.
2. J. Bhasker, *A VHDL Synthesis Primer,* Second Edition, Star Galaxy, 1998.
3. J. Bhasker, *A Verilog HDL Primer,* Second Edition, Star Galaxy, 1999.
4. J. Bhasker, *A Verilog Synthesis : A Practical Primer,* Star Galaxy, 1998.
5. M. J. S. Smith, *Application Specific Integrated Circuits*, AW/Pearson, 1997.

REFERENCE BOOKS:

1. Z. Navabi, *VHDL : Analysis and Modeling of Digital Systems,* Second Edition, MH, 1998..
2. J. Armstrong and F. G. Gray, *VHDL Design Representation and Synthesis,* Second Edition, PH/Pearson, 2000.
3. P. J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann, 2001.
4. D. Naylor and S. Jones, *VHDL : A Logic Synthesis Approach*, Chapman & Hall, 1997.

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-715	Embedded System Design

Introduction to Embedded systems design:
Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES.

8051 Microcontroller: Microprocessor V/s Micro-controller, 8051 Microcontroller: General architecture; Memory organization; I/O pins, ports & circuits; Counters and Timers; Serial data input/output; Interrupts.

8051 Instructions: Addressing Modes, Instruction set: Data Move Operations, Logical Operations, Arithmetic Operations, Jump and Call Subroutine, Advanced Instructions.

8051 Interfacing and Applications: Interfacing External Memory, Keyboard and Display Devices: LED, 7-segment LED display, LCD.

Advanced Microcontrollers: Only brief general architecture of AVR, PIC and ARM microcontrollers; JTAG: Concept and Boundary Scan Architecture.

Text Books:

1. Embedded Systems by Raj Kamal, TMH, 2006.
2. The 8051 Microcontroller by K Ayala, 3rd Ed., Thomson Delmar Learning, 2007.
3. 8051 Microcontroller by S. Ghoshal, Pearson Education, 2010.
4. The 8051 Microcontrollers by K. Uma Rao and A. Pallavi, Pearson Ed., 2009.
5. Microcontrollers by Raj Kamal, Pearson Education, 2005.
6. PIC Microcontroller by H.W Huang, Delmar CENGAGE Learning, 2007.
7. J B Peatman, Design with PIC Microcontrollers, Prentice Hall.

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ECL-719	Signal Processing

1**. Speech Processing :** Speech Communication Acoustic Theory of Speech: The Source–filter Model Speech Models and Features Linear Prediction Models of Speech Harmonic Plus Noise Model of Speech Fundamental Frequency (Pitch) Information Speech Coding, Speech Recognition

2 **Signal Processing and Auditory Perception:** Introduction , Musical Notes, Intervals and Scales Musical Instruments Review of Basic Physics of Sounds Music Signal Features and Models Anatomy of the Ear and the Hearing Process Psychoacoustics of Hearing ,Music Coding (Compression)

High Quality Audio Coding: MPEG Audio

3 **Time Delay Estimation:** Need for the Time Delay Estimation, System Model, Source Localization strategies,Ideal Model-Free field environment, TDE METHODS: Cross-correlation Function(CCF) method ,Least mean square (LMS) adaptive filter method ,Average square difference function (ASDF) method , Relation between the SNR level and the time delay estimation.

4. **Channel Equalization and Blind Deconvolution :**Introduction and need For Channel Equalization , Types of Equalization Techniques , Decision Feedback Equalization Non-blind Equalization Linear Equalization Blind Equalization General Mathematical Model , Channel Modeling and algorithms

5. **System modeling and identification**: System identification based on FIR (MA), All Pole (AR), Pole Zero (ARMA) system models, Least square linear prediction filter, FIR least squares inverse filter, predictive de convolution, Matrix formulation for least squares estimation: Cholesky decomposition, LDU decomposition, QRD decomposition, Grahm V Schmidt orthogonalization.

BOOKS:

1. Siomon S Haykins, "Adaptive Filter Theory,"PHI, 3rd Edition
2. Proakis,"Digital Signal Processing,"PHI 2nd edition
3. Harry L. Van Trees, "

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ECP-716	**Digital VLSI Design Lab**

Experiments related to theory ECL-713.

ECP-717	**HDL Lab**

Experiments related to theory ECL-714.

ECP-718	**Embedded System Design Lab**

Experiments related to theory ECL-715.

SECOND SEMESTER

ECL-721	MOBILE COMMUNICATION

Introduction to Wireless Communication Systems: Various Generations of wireless mobile communication, The Cellular Concept, Frequency reuse, channel assignment strategies, hand-off strategies, interference and system capacity, improving capacity of cellular system through cell splitting, sectoring, etc.

Mobile Radio Propagation: Introduction to radio wave propagation, three basic propagation mechanisms, Outdoor & indoor propagation models, small scale multipath propagation, parameters of mobile multipath channel, small scale & large scale fading, their types.

Principles of GSM: GSM frequency bands, GSM architecture, GSM Interfaces, GSM logical channels and frame structure, GSM bursts, GPRS.

CDMA System Concepts: Basics of CDMA. Spread spectrum concept. time hopping, Direct Sequence and Frequency Hopped Spread Spectrum, Chirp spread spectrum systems, Hybrid systems, Spreading sequences and their correlation functions, Code generation, Properties and generation of PN sequences, RAKE receiver, Diversity techniques an Rake receiver, Soft handoffs.

Implementation Issues: OFDM, Multi-Carrier Modulation and Demodulation, Channel Coding and Decoding (Convolutional codes, Turbo codes), Multi-user Detection: Decorrelating detector, MMSE detector. Successive Interference Canceller, Parallel Interference Canceller.

Text Books:

1. Mobile Cellular Telecommunications; 2nd ed.; William, C Y Lee McGraw Hill
2. Wireless and Digital Communications; Dr. Kamilo Feher (PHI)
3. Principles of Mobile Communication, G.LStuber Kluwer Academic, 1996
4. Wireless Communication; Principles and Practice; T.S.Rappaport

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ECL-722	Advanced Optical Communication Systems

Review: Evolution of Basic Fiber Optic Communication System, Benefits and disadvantages of Fiber Optics, Transmission Windows, Transmission Through Optical Fiber, The Numerical Aperture (NA), The Optical Fiber, Types of Fiber, Different Losses & Issues in Fiber Optics, Attenuation in Optical Fibers, Fiber Optic Loss Calculations, Dispersion, connectors & splices, bending loses, Absorption, scattering, very low loss materials, plastic & polymer-clad-silica fibers. Wave propagation in step index & graded index fiber, fiber dispersion, single mode fibers, multimode fibers, dispersion shifted fiber, dispersion flattened fiber, polarization, cut-off condition and V-parameter.

Fiber Optic System Design Considerations and Components Components: Indoor Cables, Outdoor Cables, Cabling Example, Power Budget, Bandwidth and Rise Time Budgets, Electrical and Optical Bandwidth, Connectors, Fiber Optic Couplers.

Dispersion and Nonlinearities Dispersion in single mode and multimode fibers, dispersion shifted and dispersion flattened fibers, attenuation and dispersion limits in fibers, Kerr nonlinearity, self phase modulation, Cross Phase Modulation, FWM.

Optical Sources: optical source properties, operating wavelength of optical sources, semiconductor light-emitting diodes and laser diodes, semiconductor material and device operating principles, light-emitting diodes, surface-emitting LEDS, edge-emitting LEDS, super luminescent diodes, laser diodes, comparison of LED and ILD. Fiber optic transmitters, basic optical transmitters, direct versus external modulation, fiber optic transmitter applications.

Optical Detectors: Basic Information on light detectors, Role of an optical detector, Detector characteristics: Responsivity, Noise Equivalent Power, Detectivity, Quantum efficiency, The PN junction photo diode - PIN photodetectors - Avalanche photo diode construction characteristics and properties, APD Specifications, Applications of APD, Optical Receivers

Advanced Multiplexing Strategies: Optical TDM, subscriber multiplexing (SCM), WDM and Hybrid multiplexing methods.

Optical Networking: Data communication networks, network topologies, MAC protocols, Network Architecture- SONET/TDH, optical transport network, optical access network, optical premise network

Books:

1. G.P Aggrawal, Fiber-Optic Communication Systems, Wiley-interscience
2. G. Keiser, Optical Fiber Communication, Tata –McGraw Hill.
3. John Gowar , Optical communication systems, PHI.

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ECL-723	Analog IC Design

Small Signal & large signal Models of MOS & BJT transistor.
MOS & BJT Transistor Amplifiers: Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers
Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode. Differential Amplifiers: Differential pair & DC transfer characteristics.
Current Mirrors, Active Loads & References
Current Mirrors: Simple current mirror, Cascode current mirrors Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques.

Operational Amplifier: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Bipolar operational amplifiers. Frequency response & compensation.

Nonlinear Analog Circuits: Voltage controlled oscillator, Comparators, Analog Buffers, Source Follower and Other Structures. Phase Locked Techniques; Phase Locked Loops (PLL), closed loop analysis of PLL. Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters.

OTA & Switched Capacitor filters

OTA Amplifiers, Switched Capacitor Circuits and Switched Capacitor Filters.

Text:

1. Paul B Gray and Robert G Meyer, "Analysis and Design of Analog Integrated Circuits".
2. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.

References:

1. D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley, 1997.
2. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
3. Behzad Razavi, "Principles of data conversion system design", S.Chand and company Ltd, 2000. John Wiley
4. Kenneth R. Laker, Willy M.C. Sensen, " Design of Analog Integrated circuits and systems", McGraw Hill, 1994.

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ECL-724	Adaptive Signal Processing

Basic Of Digital Signal Processing: Signals and Information, Signal Processing Methods, Applications of Digital Signal Processing, Derivation of the z-Transform Properties of z-Transform, Fourier series and Fourier transform., Random variable, Stochastic processes.

2.**Design Of Digital Filters:** Introduction, Linear Time-Invariant Digital Filters, Recursive and Non-Recursive Filters, Filtering Operation, Sum of Vector Products, A Comparison of Convolution and Correlation, Filter Structures, Direct, Cascade and Parallel Forms, Linear Phase FIR Filters Design of Digital FIR Filter-banks, Sub-band Filters, Design of Infinite Impulse Response IIR filters, Issues in the Design and Implementation of a Digital Filter.

3.**Estimation Theory**: Bayesian Estimation Theory, Basic Definitions, Bayesian Estimation, Expectation Maximization Method, Generalized Parameter Estimation,Cramer–Rao lower Bound on the variance of estimator, maximum likelihood estimation, Design of Gaussian Mixture Models , Bayesian Classification, Modeling the Space of a Random Process, Detection

4. **AdaptiveFiltering:**State-Space Kalman Filters,Recursive Least Square (RLS) Adaptive Filters The Steepest-Descent Method LMS Filter, Different Algorithms and their Variants used in adaptive filtering and their performance criteria.Multirate Signal Processing

5. **Applications:** Applications of adaptive Digital Signal Processing to Speech, Music and Telecommunications, Parameter estimation, System identification, Noise and Echo cancellation, Acoustic source localization techniques, Channel Equalization.

BOOKS:

1. Siomon S Haykins, "Adaptive Filter Theory,"PHI, 3rd Edition

2. Proakis,"Digital Signal Processing,"PHI 2nd edition

3. Harry L. Van Trees, " Detection, Estimation, and Modulation Theory, Part 1&3," Wiley 2002

4.Saeed V. Vaseghi, "Advanced Digital Signal Processing and Noise Reduction," Third Edition,2006

5. Eberhard Hänsler, "Gerhard Schmidt Acoustic Echo and Noise Control: A Practical Approach,"wiley,2005

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ELECTIVE-I

The student can opt any one elective from the following list.

ECL-725 (i)	Algorithm for VLSI Design Automation

Logic synthesis & verification:

Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

VLSI automation Algorithms:

Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor plannning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text Books:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

References

1. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
2. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition
3. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-725(ii)	Advanced Computer Architectures

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors .**Pipelining:** Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,

Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.

Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine check, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.

Text:

1. Kai Hwang, "Advanced computer architecture"; TMH.

2. D. A. Patterson and J. L. Hennessey, "Computer organization and design," Morgan Kaufmann, 2nd Ed.

References:

1. J.P.Hayes, "computer Architecture and organization"; MGH.
2. Harvey G.Cragon,"Memory System and Pipelined processors"; Narosa Publication.
3. V.Rajaranam & C.S.R.Murthy, "Parallel computer"; PHI.

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ECL-725 (iii)	**MEMS and IC Integration**

Overview of CMOS process in IC fabrication, MEMS system-level design methodology, Equivalent Circuit representation of MEMS, signal-conditioning circuits, and sensor noise calculation.

Pressure sensors with embedded electronics(Analog/Mixed signal): Accelerometer with transducer, Gyroscope,RF MEMS switch with electronics, Bolo meter design.

RF MEMS, and Optical MEMS

Text/References:

1. Gregory T.A. Kovacs, Micromachined Transducers Sourecbook, The McGraw-Hill, Inc. 1998
2. Stephen D. Senturia, Microsystem Design, Kluar Publishers, 2001
3. Nadim Maluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2000.
4. M.H. Bao, Micro Mechanical Transducers, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000.
5. Masood Tabib-Azar, Microactuators, Kluwer, 1998.
6. Ljubisa Ristic, Editor, Sensor Technology and Devices, Artech House, 1994
7. D. S. Ballantine, et. al., Acoustic Wave Sensors, Academic Press, 1997
8. H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech, 1999.
9. James M.Gere and Stephen P. Timoshenko, Mechanics of Materials, 2nd Edition, Brooks/Cole Engineering Division, 1984

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ECP-726	Adaptive Signal Processing Lab

List of Experiments:
1. Write matlab statement for algebraic equations.
2. Designing Filters from Windowing techniques.
3. Write matlab programme to find the Power spectral Density.
4. Matlab Programme for Ploting different Graphs.
5. Filter design with the help of matlab filter design tool.
6. Simulation of the given model using Simulink tool.
7 Matlab programme for cross correlation and auto correlation .
8. Working with DSP Processor &Hardware.

ECP-727	Advanced Communication Lab

Experiments related to theory of subjects related to communication engineering.

THIRD SEMESTER

ELECTIVE-II

The student can opt any one elective from the following list.

ECL-731 (i)	Mixed-Signal Design

1. Passive and Active Parameter Sensitivity and Component Ratioing.
2. Analog Filters (Continuous-Time and Switched-Capacitor); Digital Filters.
3. Sample-and-Hold Circuits.
4. Analog-to-Digital Converters; Digital-to-Analog Converters.
5. Sigma-Delta Converters.

TEXT BOOK:

1. R. J. Baker, *CMOS Mixed Signal Cicuit Design*, Wiley/IEEE, 2002.

REFERENCE BOOKS:

1. A. Handkiewicz, *Mixed-Signal Systems : A Guide to CMOS Circuit Design*, Wiley-IEEE, 2002.
2. P. V. A. Mohan, V. Ramachandran and M. N. S. Swamy, *Switched Capacitor Filters : Theory, Analysis and Design*, PH, 1995.
3. E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed-Signal Circuits*, IEEE, 1999.
4. E. N. Farag and M. I. Elmasry, *Mixed-Signal VLSI Wireless Design : Circuits and Systems*, Kluwer, 1999.
5. R. Schaumann and M. E. Valkenburg, *Design of Analog Filters*, OUP, 2001.
6. Y. Tsividis, *Mixed Analog-Digital VLSI Devices and Technology*, MH, 1996.
7. R. Unbehauen and A. Cichocki, *MOS Switched Capacitor and Continuous-Time ICs and Systems*, Springer-Verlag, 1989.
8. S. R. Norsworthy, R. Schreier and G. C. Temes, *Delta-Sigma Data Converters : Theory, Design and Analysis*, IEEE, 1996.
9. F. Medeiro, B. Perez-Verd and A. Rodroguez-Vazquez, *Top-Down Design of High-Performance Sigma-Delta Modulators*, Kluwer, 1998.
10. V. Peluso, M. Steyaert and W. M. C. Sansen, *Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters*, Kluwer, 1999.
11. S. Rabii and B. A. Wooley, *Design of Low-Voltage Low-Power Sigma-Delta Modulators*, Kluwer, 1998.
12. P. G. A. Jespers, *Integrated Converters : D-A and A-D Architectures, Analysis and Simulation*, OUP, 2001.
13. R. Van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer, 1994.
14. B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.

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ECL-731 (ii)	RF Micro-electronics

Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology.

Basic concepts in RF Design: Nonlinearly and Time Variance, intersymbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.

Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection. Mobile RF Communication systems and basics of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation.

Basic blocks in RF systems and their VLSI implementation : Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design. Quadrature and single-sideband generators.

Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques, Design issues in integrated RF filters.

Some discussion on available CAD tools for RF VLSI designs.

Texts/References:

1. B.Razavi, RF Microelectronics, Prentice-Hall PTR,1998
2. T.H.Lee, The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 1998.
3. R.Jacob Baker,H.W.Li, and D.E. Boyce, CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of India,1998.
4. Y.P. Tsividis Mixed Analog and Digital VLSI Devices and Technology, McGraw Hill,1996

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-731 (iii)	VLSI Testing & Testability

The need for testing, the problems of digital and analog testing, Design for test, Software testing

Faults in Digital circuits:General introduction, Controllability and Observability.. Fault models - Stuck-at faults, Bridging faults, intermittent faults

Digital test pattern generation :Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D-algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits , Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing

Signatures and self test: Input compression Output compression Arithmetic, Reed-Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients ,Spectral coefficients, Coefficient test signatures ,Signature analysis and Online self test

Testability Techniques : Partitioning and ad hoc methods and Scan-path testing , Boundary scan and IEEE standard 1149.1 ,Offline built in Self Test (BIST), Hardware description languages and test

Testing of Analog and Digital circuits : Testing techniques for Filters, A/D Converters, RAM, Programmable logic devices and DSP

Text:

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub:Inspec/IEE ,1999

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-731 (iv)	Memory System Design

Introduction to Memory Chip Design: Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Basic Operation of The 1-T Cell, Basic Operation of a SRAM Cell, Trends in Non-Volatile Memory Design and Technology, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology,

Basics of RAM Design and Technology: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.

DRAM Circuits: High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, W rite and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.

On-Chip Voltage Generators: Substrate-Bias Voltage (VBB) Generator, Voltage Up-Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.

High-Performance Subsystem Memories: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.

Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.

Ultra-Low-Voltage Memory Circuits: Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low-Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-731 (v)	Low Power VLSI Design

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation

Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. **Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library **Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution : Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & architectural level methodologies : Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002

2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997

References:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-731 (vi)	Embedded System for Wireless & Mobile Communication

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol

Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping

Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatternet

Connection establishement procedure, notable aspects of connection establishement, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile, Secondary bluetooth profile

Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers

Programming with Java: Java Programming, J2ME architecture, Javax.bluetooth package Interface, classes, exceptions, Javax.obex Package: interfaces, classes

Bluetooth services registration and search application, bluetooth client and server application.
Overview of IrDA, HomeRF, Wireless LANs, JINI

Text:

1. Bluetooth Technology by C.S.R. Prabhu and A.P. Reddi; PHI

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-731 (vii)	Hardware & Software Co-Design

Introduction :Motivation hardware & software co-design, system design consideration, research scope & overviews **Hardware Software back ground**: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development,

Hardware Software co-design research : An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment.

Co-design concepts :Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software trade offs, co-design.

Methodology for co-design : Amount of unification, general consideration & basic philosophies, a framework for co-design.

Unified representation for Hardware & Software : Benefits of unified representation, modeling concepts

An abstract Hardware & Software model : Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model

Performance evaluation: Application of t he abstract Hardware & Software model, examples of performance evaluation

Object oriented techniques in hardware design: Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.

Text

1. Sanjaya Kumar, James H. Ayler "The Co-design of Embedded Systems: A Unified Hardware Software Representation", Kluwer Academic Publisher, 2002

References

1. Gomaa, Software Design Methods for Concurrent and Real-time Systems, Addison-Wesley, 1993.
2. H. Kopetz, Real-time Systems, Kluwer, 1997.
3. R. Gupta, Co-synthesis of Hardware and Software for Embedded Systems, Kluwer 1995.
4. S. Allworth, Introduction to Real-time Software Design, Springer-Verlag, 1984.
5. C. M. Krishna, K. Shin, Real-time Systems, Mc-Graw Hill, 1997.
6. Peter Marwedel, G. Goosens, Code Generation for Embedded Processors, Kluwer Academic Publishers, 1995.

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-731 (viii)	Advanced Digital Communication

Introduction: Elements of Digital Communication system, Bandpass and Lowpass signal representation, Comparison between analog & Digital Communication, Performance parameters of Digital Communication, Concept of Constellation, BER, etc.

Digital Modulation Techniques: Mathematical expressions, transmitter & receiver structure of ASK, FSK, BPSK, QPSK, M-ary PSK, MSK, QAM.

Reception of Digital Signal: Baseband signal reception, Probability of error, Optimum filter receiver, Matched filter receiver, Coherent reception, calculation of error probability for PSK, MSK, ISI, Pulse Shaping Techniques.

Information Theory & Coding: Measures of information, Entropy, Information rate, Channel Capacity, Source Coding (Huffman, Shannon-Fano, Lempel-Ziv), Channel coding (Block codes, Convolution codes, Turbo codes).

Books:

1. Digital Communications by J.G Proakis & M Salehi, 5th Edition McGraw Hill
2. Principle of Communication systems –Taub & Schilling,Tata Mc Graw Hill
3.Digital Communication –Simon Haykins , John Wiley & Sons.
4. Digital Communications: Fundamentals and applications- Bernard Sklar, PHI
5. B.P.Lathi,Modern Digital and analog communication systems,3rd Edition, Oxford University *Press,1998.*

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-731 (ix)	Satellite Communication

1. Orbital Parameters:

Orbital parameters, Orbital perturbations, Geo stationary orbits, Low Earth and Medium orbits. Frequency selection, Frequency co-ordination and regulatory services, Sun transit outages, Limits of visibility, Attitude and orientation control, Spin stabilization techniques, Gimbal platform

2. Link Calculations:

Space craft configuration, Payload and supporting subsystems, Satellite uplink -down link power budget, C/No, G/T, Noise temperature, System noise, Propagation factors, Rain and ice effects, Polarization calculations

3. Access Techniques:

Modulation and Multiplexing: Voice, Data, Video, Analog and Digital transmission systems, multiple access techniques: FDMA, TDMA, T1-T2 carrier systems, SPADE, SS-TDMA, CDMA, Assignment Methods, Spread spectrum communication, Compression-Encryption and Decryption techniques

4. Earth Station Parameters:

Earth station location, propagation effects of ground, High power transmitters-Klystron Crossed field devices, Cassegrania feeds, Measurements on G/T and Eb/No

5. Satellite Applications:

INTELSAT Series, INSAT, VSAT, Remote sensing, Mobile satellite service: GSM. GPS, INMARSAT, Satellite Navigation System, Direct to Home service (DTH), Special services, E-mail, Video conferencing and Internet connectivity

Books:

1. Bruce R. Elbert," The Satellite Communication Applications Hand Book, Artech House Boston, 1997
2. Wilbur L.Pritchard, Hendri G.Suyderhood, Robert A.Nelson, "Satellite Communication Systems Engineering" ,IIEdition, Prentice Hall, New Jersey.1993
3. Dennis Rody," Satellite Communication", Regents/Prentice Hall, Eaglewood Cliff, New Jersey, 1983
4. Tri T.Ha, "Digital satellite communication", 2nd Edition, McGraw Hill, New york.1990
5. K.Feher, Digital communication satellite / Earth Station Engineering, prentice Hall Inc, New Jersey, 1983

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

Advance VLSI Design Lab
ECP-732

List of Experiments

1. To study the characteristics of Common gate configuration in mentor graphic Design architecture.
2. To study the characteristics of Common source configuration in mentor graphic Design architecture.
3. To study the characteristics of Common drain configuration in mentor graphic Design architecture.
4. To study the characteristics of switched capacitor integrator amplifier in mentor graphic Design architecture.
5. To study the characteristics of two stage MOS OpAmp configuration in mentor graphic Design architecture.
6. To study the characteristics of MOS Cascode configuration in mentor graphic Design architecture.
7. To study the characteristics of MOS Folded-cascode operational amplifiers configuration in mentor graphic Design architecture.
8. To study the characteristics of Source Follower configuration in mentor graphic Design architecture.
9. To study the characteristics of OTA Amplifiers configuration in mentor graphic Design architecture.
10. To study the characteristics of Voltage controlled oscillator and Comparators, configuration in mentor graphic Design architecture.
11. Design of VCO, DCOs and PLL circuits.
12. Layout design of circuits and verification of designs through simulation.

Communication System Design Lab
ECP 733

Experiments related to communication system designs using OPTSIM/MATLAB software.

ECD-730	**Thesis – Part I**

The Thesis work should be of Research nature only and it should be started during the third semester and the candidate must do the following:

1. Literature Survey
2. Problem Formulation

Around 40% of the Thesis work should be completed in this semester. The remaining 60% work will be carried out in the fourth semester. Each student is required to submit a detailed report about the work done on topic of Thesis as per the guidelines decided by the department. The Thesis work is to be evaluated through Presentations and Viva-Voce

during the semester and at the end of semester as per the guidelines decided by the department from time to time.

FOURTH SEMESTER

ECD-740	Thesis – Part II

Around 40% of the Thesis work should be completed in third semester. The remaining 60% work will be carried out in this semester. Each student is required to submit a detailed Thesis report about the work done (III Sem + IV Sem) on topic of Thesis as per the guidelines decided by the department. The Thesis work is to be evaluated through Presentations and Viva-Voce during the semester and Final evaluation will be done at the end of semester as per the guidelines decided by the department from time to time.

The candidate has to present/publish one paper in national/international conference/seminar/journal of repute is must before submission. Research work should be carried out at GJUS & T, Hisar. However candidate may visit research labs/institutions with the due permission of chairperson on recommendation of supervisor concerned.